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Dated: April 29, 2009 Signature: /Laura C. Brutman (Laura C. Brutman)

Docket No.: J0658.0018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jens Barrenscheen et al.

Application No.: 10/727,102 Confirmation No.: 4397

Filed: December 2, 2003 Art Unit: 2181

For: Arrangement comprising a first semiconductor chip and a second semiconductor chip connected thereto Examiner: C. K. Lee

APPEAL BRIEF SUBMITTED IN RESPONSE TO THE NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is filed within one month of the Notification of Non-Compliant Appeal Brief mailed on April 17, 2009.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Argument

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

INFINEON TECHNOLOGIES AG

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 22 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 1, 5 and 21
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 2-4, 6-20 and 22-25
4. Claims allowed: None
5. Claims rejected: 2-4, 6-20 and 22-25

C. Claims On Appeal

The claims on appeal are claims 2-4, 6-20 and 22-25

IV. STATUS OF AMENDMENTS

Applicants filed an Amendment in response to an Advisory Action mailed on August 30, 2007. The Examiner responded in a Non-Final Office Action mailed on November 14, 2007. Applicants responded on March 13, 2008, and, subsequently, the Examiner mailed a Final Rejection on April 15, 2008, from which Applicants appeals. As such, the claims in Appendix A incorporate the amendments indicated in the papers filed by Applicants on August 30, 2007.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claims 23-25 are independent. As shown below, each limitation is disclosed by at least the following citations to the Specification and Figures. Specification citations are provided in accordance with 37 C.F.R. § 41.37, such reference numerals and citations are merely examples of where support may be found in the specification. There is no intention to suggest in any way that the terms of the claims are limited to the examples in the specification or the specific citations used. As demonstrated by the reference numerals and citations above, the claims are fully supported by the specification as required by law. However, it is improper under the law to read limitations from the specification into the claims. The reference numerals and specification citations are not to be construed as claim limitations or in any way used to limit the scope of the claims.

A. Claim 23:

23. An arrangement (see Fig. 2; pg. 9, lns. 6-9) comprising:

a first semiconductor chip (MCN; pg. 9, lns. 19-25); and

a plurality of second semiconductor chips (see, e.g., PCN as one of plurality) which are connected to and drives electrical loads based on a timing defined by load control data (pg. 14, lns. 17-26);

a first data line (SD1) via which the second semiconductor chip (PCN) transmits diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip (PCN), to the first semiconductor chip (MCN) (pg. 11, lns. 3-7);

a chip select line (EN) associated with each of the second semiconductor chips (pg. 14, lns. 7 – pg. 15, ln. 9); and

a single, second data line (SO) via which the first semiconductor chip (MCN) transmits the load control data and pilot data which control the second semiconductor chips (PCN) (pg. 10, lns. 19-25);

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing (pg. 10, lns. 25-27; pg. 11, ln. 8 – pg. 12, ln. 17); and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip (see, e.g., PCN), and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip as designated by data on the chip select line (EN) (pg. 14, ln. 17 – pg. 15, ln. 22).

B. Claim 24:

24. An arrangement (see Fig. 2; pg. 9, lns. 6-9) comprising:

a first semiconductor chip (MCN; pg. 9, lns. 19-25); and

a plurality of second semiconductor chips (see, e.g., PCN as one of plurality) which are connected to and drives electrical loads based on a timing defined by load control data (pg. 14, lns. 17-26);

a chip select line (EN) associated with each of the second semiconductor chips (pg. 14, lns. 7 – pg. 15, ln. 9);

a first data communication means (SD1) for the second semiconductor chip (PCN) transmitting diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip (PCN), to the first semiconductor chip (MCN) (pg. 11, lns. 3-7); and

a single, second data communication means (SO) for the first semiconductor chip (MCN) transmitting the load control data and pilot data which control the second semiconductor chip (PCN) (pg. 10, lns. 19-25),

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing (pg. 10, lns. 25-27; pg. 11, ln. 8 – pg. 12, ln. 17); and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip as designated by data on the chip select line (EN) (pg. 14, ln. 17 – pg. 15, ln. 22).

C. Claim 25

25. A method for communicating in an arrangement having a first semiconductor chip (MCN) and a plurality of second semiconductor chips (see, e.g., PCN as one of plurality) which are connected to and drives electrical loads based on a timing defined by load control data (pg. 14, lns. 17-26), comprising:

the second semiconductor chip (PCN) transmitting diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip, via a first data line (SD1) to the first semiconductor chip (MCN) (pg. 11, lns. 3-7); and

the first semiconductor chip (MCN) transmitting the load control data and pilot data, which control the second semiconductor chips (PCN), via a single, second data line (SO) (pg. 10, lns. 19-25),

transmitting a chip select signal (EN) on a chip select line (pg. 14, lns. 7 – pg. 15, ln. 9),

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing (pg. 10, lns. 25-27; pg. 11, ln. 8 – pg. 12, ln. 17); and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip as designated by data on the chip select line (EN) (pg. 14, ln. 17 – pg. 15, ln. 22).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The rejection of claims 2-4, 6-8, 10, 12, and 23-25 under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of U.S. Patent Publication No. 2003/0103519 ("Balasundram").

The rejection of claim 9 under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view Balasundram in further view of U.S. Patent No. 3,985,962 ("Jones").

The rejection of claims 11, 15 and 17 under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view Balasundram in further view "Data Communication Basics".

The rejection of claims 13-14 and 22 under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view Balasundram in further view of U.S. Patent No. 6,772,251 ("Hastings").

The rejection of claim 16 under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view Balasundram in further view of "Data Communication Basics" and U.S. Patent No. 6,154,509 ("Bishop").

The rejection of claims 18-20 under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view Balasundram in further view of U.S. Patent No. 6,578,940 ("Rehmann").

VII. ARGUMENT

Claims 2-4, 6-20 and 22-25 are pending and have been examined in the present application. Claims 23-25 are independent and claims 2-4, 6-20 and 22 depend from and include all of the limitations of claim 23. All of the claims are in condition for allowance and any pending rejections should be withdrawn.

A. Claims 2-4, 6-8, 10, 12, and 23-25 Are Patentable Over AAPA in view of Balasundram

Claims 2-4, 6-8, 10, 12, and 23-25 stand improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of U.S. Patent Publication No. 2003/0103519 ("Balasundram"). Claims 23-25 are independent. Appellants respectfully submit that the Board must order the withdrawal of these rejections.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or combine references to arrive at the claimed subject matter. The prior art references must also teach or suggest all the limitations of the claim in question. See M.P.E.P. § 706.02(j). A reference can only be used for what it clearly discloses or suggests. See In re Hummer, 113 U.S.P.Q. 66 (C.C.P.A. 1957); In re Stencel, 4 U.S.P.Q.2d 1071, 1073 (Fed. Cir. 1987).

Here, the references, whether taken individually or in combination, do not disclose or suggest the invention claimed by Appellants. More particularly, the cited references do not disclose that "a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip," as required by each of independent claims 23-25.

The Examiner has acknowledged that the AAPA does not disclose this feature and looks to Balasundram to cure the AAPA's deficiency, citing, for example, paragraphs [0008] and [0046] of Balasundram. Paragraph [0008] discloses that each transmitter receiver pair is allocated a particular time interval or channel for its data. Moreover, paragraph [0046] discloses that the data signals are sent through a series of time intervals using multiple byte waveform technology. As such, neither cited portion of Balasundram reads on the explicitly recited limitation of independent claims 23-25.

Rather, as provided in Balasundram, each multiple byte waveform message has a fixed leading byte, *i.e.*, an identifier address, that signifies the start of each message. "This is an identifier address that is unique to the communicating transmitter and receiver pairs and ensures that the receiver ignores all signals not preceded by this address." (See paragraph [0039] of Balasundram.) As a result, any data in a given multiple byte waveform message is received by only the receiver that recognizes the specific identifier address.

Accordingly, Balasundram does not teach or suggest a portion of data on a frame is intended for a first, second semiconductor chip, and a portion of data on the same frame is intended for a second, second semiconductor chip, as required by the independent claims. Inherently, because each of Balasundram's multiple byte waveform messages has a fixed leading byte, Balasundram does not disclose that a plurality of data is transferred utilizing a single allotted time interval (e.g., a single frame), as previously asserted by the Examiner. Therefore, Balasundram fails to read on the explicitly recited limitation.

Appellants note that each reference is not being addressed individually, but that the combination of the two references is deficient in that they do not disclose what is recited by independent claims 23-25. However, Appellants further submit that one of ordinary skill in the art would not have been motivated to combine these two references to arrive at the claimed invention.

The Examiner has contested that one skilled in the art would have combined the AAPA with Balasundram to reduce the size, cost, and complexity of the system thereby reducing the overall number of wires needed in a multisystem application situation. Appellants respectfully disagree. As discussed above, Balasundram discloses a time-division multiplexing system that requires a header, *i.e.*, an identifier address, associated with the data to designate the destination for the data. The pending claims of the present application explicitly recite that the data is transmitted in frames using data on a chip select line. The claimed chip select line designates the load control data and pilot data frames for a specific address, whereas the chip

select line in the prior art is designated at the beginning and the end of the data transmission. Thus, even if one were to combine the two references, one would not arrive at the explicitly recited claims invention. However, because Balasundram requires a header to associate the data with the designated address, one skilled in the art would also not look to Balasundram for any additional teaching with respect to the prior art.

Accordingly, for at least these reasons, Appellants maintain that independent claims 23-25 are patentable over the prior art of record. As such, the rejection of these independent claims must be reversed.

Moreover, claims 2-4, 6-8, 10 and 12, depend either directly or indirectly from, and contain all the limitations of independent claim 23. These dependent claims also recite additional limitations, which, in accommodation with the limitations of the independent claims, are not disclosed nor suggested by the AAPA in view of Balasundram. Accordingly, Appellants are not arguing these rejections separately from the arguments in response to the rejections of claims 23-25 discussed above. As such, Appellants are not required to submit a concise explanation for dependant claims 2-4, 6-8, 10 and 12. See 37 C.F.R. §41.37(c)(1)(v).

B. Claims 9, 11, 13-20 and 22 Are Not Unpatentable Under 35 U.S.C. § 103(a)

With respect to the rejections of dependent claims 9, 11, 13-20 and 22 under 35 U.S.C. § 103(a), Appellants note that the additional references are cited for their disclosure of additional limitations, which, even if they were to show, do not cure the deficiencies in the AAPA and Balasundram as discussed above. Therefore, all of these pending dependent claims are also in immediate condition for allowance. Appellants are also not arguing these rejections separately, and, therefore, Appellants are not required to submit a concise explanation for these dependant claims pursuant to 37 C.F.R. §41.37(c)(1)(v).

C. Conclusion

For the reasons discussed above, Appellants respectfully request that the board order the withdrawal of the rejections for pending claims 2-4, 6-20 and 22-25.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Applicant on August 30, 2007.

Dated: April 29, 2009

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/727,102

2. The arrangement as claimed in claim 23, wherein the first semiconductor chip is a program-controlled unit.

3. The arrangement as claimed in claim 23, wherein the second semiconductor chip is a power chip.

4. The arrangement as claimed in claim 23, wherein the second data line is part of a second transmission channel which comprises:

a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip;

the second data line, via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal; and

a chip select line via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip, the chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the second data line.

6. The arrangement as claimed in claim 23, wherein the first semiconductor chip defines time windows of constant length and transmits in each time window either a load control data frame or a pilot data frame or no data.

7. The arrangement as claimed in claim 6, wherein the first semiconductor chip transmits no further load control data frame for a respective length of n time windows after transmission of a load control data frame, where $n \geq 0$ and where n can be set by the user of the arrangement.

8. The arrangement as claimed in claim 7, wherein a pilot data frame can be transmitted only in a time window in which no load control data frame is to be transmitted.

9. The arrangement as claimed in claim 6, wherein transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously.

10. The arrangement as claimed in claim 23, wherein the first data line is part of a first transmission channel, and the first data line is used to transmit neither load control data nor pilot data.

11. The arrangement as claimed in claim 23, wherein the diagnostic data are transmitted in synch with a transmission clock signal generated in the second semiconductor chip, and wherein this transmission clock signal is not transmitted to the first semiconductor chip.

12. The arrangement as claimed in claim 23, wherein the first semiconductor chip transmits appropriate pilot data in order to prescribe to the second semiconductor chip what transmission rate is to be used by the second semiconductor chip to transmit the diagnostic data to the first semiconductor chip.

13. The arrangement as claimed in claim 12, wherein the transmission rate is prescribed by transmitting a division factor, and wherein the second semiconductor chip divides the frequency of a transmission clock signal transmitted to it by the first semiconductor chip by the division factor and transmits the diagnostic data to the first semiconductor chip in time with the resultant signal.

14. The arrangement as claimed in claim 13, wherein the transmission clock signal supplied to the second semiconductor chip represents the transmission clock which is used by the first semiconductor chip to transmit the load control data or the pilot data to the second semiconductor chip.

15. The arrangement as claimed in claim 11, wherein the diagnostic data are transmitted in units of frames, where a frame starts with a start bit having a prescribed value and ends with one or two stop bits having prescribed values.

16. The arrangement as claimed in claim 11, wherein the first semiconductor chip ascertains the phase of the diagnostic data by oversampling the diagnostic data.

17. The arrangement as claimed in claim 23, wherein the first data line is part of a first transmission channel comprising a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip, or the second semiconductor chip transmits a transmission clock signal to the first semiconductor chip, and wherein the second semiconductor chip transmits the diagnostic data in synch with this transmission clock signal.

18. The arrangement as claimed in claim 23, wherein the second line is part of a second transmission channel which further comprises:

a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip;

a second transmission clock line via which the first semiconductor chip transmits a complementary transmission clock signal to the second semiconductor chip;

a third data line via which the first semiconductor chip transmits complementary load control data and complementary pilot data to the second semiconductor chip; and

a chip select line via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip, the chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the second data line.

19. The arrangement as claimed in claim 18, wherein output drivers on the first semiconductor chip, which output the load control data, the pilot data and the transmission clock signal, are LVDS drivers whose use limits electromagnetic interference.

20. The arrangement as claimed in claim 23, wherein the first semiconductor chip has a plurality of respective different output drivers for outputting the load control data, the pilot data and a transmission clock signal, and wherein a user of the arrangement is able to set which of the plurality of different output drivers needs to be used in each case.

22. The arrangement as claimed in claim 23, wherein the first semiconductor chip is connected to a plurality of second semiconductor chips, every second semiconductor chip is connected to the first semiconductor chip via a dedicated chip select line, and chip select signals transmitted via the chip select lines can be altered during transmission of a frame.

23. An arrangement comprising:

a first semiconductor chip; and

a plurality of second semiconductor chips which are connected to and drives electrical loads based on a timing defined by load control data;

a first data line via which the second semiconductor chip transmits diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip, to the first semiconductor chip;

a chip select line associated with each of the second semiconductor chips; and

a single, second data line via which the first semiconductor chip transmits the load control data and pilot data which control the second semiconductor chips;

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing; and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip as designated by data on the chip select line.

24. An arrangement comprising:

a first semiconductor chip; and

a plurality of second semiconductor chips which are connected to and drives electrical loads based on a timing defined by load control data;

a chip select line associated with each of the second semiconductor chips;

a first data communication means for the second semiconductor chip transmitting diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip, to the first semiconductor chip; and

a single, second data communication means for the first semiconductor chip transmitting the load control data and pilot data which control the second semiconductor chip,

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing; and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip as designated by data on the chip select line.

25. A method for communicating in an arrangement having a first semiconductor chip and a plurality of second semiconductor chips which are connected to and drives electrical loads based on a timing defined by load control data, comprising:

the second semiconductor chip transmitting diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip, via a first data line to the first semiconductor chip; and

the first semiconductor chip transmitting the load control data and pilot data, which control the second semiconductor chips, via a single, second data line,

transmitting a chip select signal on a chip select line,

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing; and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip as designated by data on the chip select line.

APPENDIX B

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.